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APPLICATIONS AND USES

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15

Active Matrix LC Displays

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15.1 INTRODUCTION

In the last few years the liquid crystal (LC) technology has made significant progress in expanding the size, resolution and performance of matrix addressed LC displays. Multiplexed twisted nematic (TN) LC cells of up to 200 lines[1] have been demonstrated. Multiplexed super twisted nematic (STN) LC color displays of up to 768 lines are available

in the market[2]. However, severe limitations in cell performance such as response time, viewing angle and grey scale operation at elevated temperatures still exist. The ultimate preferred solution for large area, high information content, color, grey-scale display applications is still the active-matrix (AM) LC approach. A comparison in performance between AM LC cells and simple multiplexed LC cells is shown in Table 15.1. Presently, consumer AM LC color televisions up to 6" diagonal are available in the market. AM LC cells up to 14" diagonal have been demonstrated[3,4]. Applications of AM LC in the military avionic devices have been actively pursued[5]. Some of these devices have been designed for the next generation aircraft cockpits. The era of large-area color AM LC display is arriving. This paper will describe the development history, device operation, fabrication processes, and performance of AM LC devices. The future development trend of the device will also be discussed.

Table 15.1. A comparison in performance between AM LC and simple multiplexed cells

	Active Matrix	Simple Multiplexed
LC Mode	TN	STN
Contrast Ratio	100 : 1	15 : 1
Viewing Angle CR>5	Horizontal : $\pm 60^{o}$ Vertical : $+45^{o}$ -30^{o}	Horizontal : $\pm 30^{o}$ Vertical : $\pm 25^{o}$
Response Time	30 - 50 ms	150 ms
Multiplexed Lines	>1000	400
Grey Scale	>16	8

15.2 DEVICE HISTORY

An AM LC display incorporates an active matrix circuit in the LC cell to assist the electrical addressing of the cell. The AM circuit

has an active device in every pixel element defined by the crossover of row and column bus lines. In a broad definition, the active device in an AM LC display has often been interpreted as a device with nonlinear characteristics. The nonlinear element can be either a two-terminal or a three-terminal device. The two terminal devices for this application started in 1980 with the Ta_2O_5 MIMs[6] (metal-insulator-metal), now include ring diodes[7], back to back diodes[8], PIN diodes[9] and SiNx MIMs[10]. The three terminal devices are thin-film transistors (TFT).

The two terminal devices (or diodes) are generally considered as an intermediate approach between a direct multiplexed LC cell and a three terminal device because they have severe limitations in grey scale performance and display size due to stringent requirements on device uniformity and threshold stability. Despite some potential advantages in device simplicity and fabrication cost saving of the two terminal devices, three terminal devices have become the selected technology and have received the predominant attention in the industry. So far only one MIM small size pocket TV has appeared on the market[11]. In this paper, we will put more emphasis of our discussions on the TFT devices.

The invention of TFT dated back to 1930's when Lilienfeld was issued a U.S. Patent in 1933[12] and Heil a German Patent a year later[13]. The first working TFT was realized by Weimer at RCA in 1962[14] using CdS as the semiconductor. There was a flurry of research activities[15,16,17] around the world on TFT's and their applications in the 1960's. However, the interest faded away near the end of the decade when the Si MOS transistor established its superiority for the application in integrated circuits. The matrix circuit incorporating a field-effect transistor and a capacitor in every pixel element for the addressing of an LC display, which is still widely used today, was first reported by Lechner[18] in 1971. Fisher[19,20] et al reported on the design of a LC color TV panel in 1972. The first attempt of constructing a TFT-LC panel was reported on in 1973 by the Westinghouse group led by Brody[21] which demonstrated the switching ON and OFF of one row of

pixels in a 6"x6" 20 line-per-inch (lpi) panel.* The first fully operational TFT-LC alphanumeric panel was achieved in 1974[24] followed by the reporting of the video performance of a 6"x6" 30 lpi TFT-LC panel in 1978[25] all using CdSe. The performance of the 1978 panel is shown in Fig. 15.1. During the 1970's, the primary efforts on TFT-LC development were conducted at Westinghouse Research Laboratory using CdSe TFT's fabricated by the shadow mask technique[26] with display resolution limited to less than 50 lpi. The display resolution of CdSe TFT devices were increased to 50 lpi by a hybrid process combining shadow mask and photolithography[27,28] and to 80 lpi and 640x400 elements on an 8"x5" active area by using an all-photolithographic[29] process.

Since the beginning of the 1980's, there has been an upsurge of interest in the TFT-LC technology. This probably is due to the following reasons:

1. The availability of a-Si and poly-Si as the semiconductor material for the TFT which could utilize conventional semiconductor processing equipment for the fabrication of these devices.
2. The explosion of development of the personal and lap top computers which require a high performance flat panel display.
3. The inadequacy and limitation of the performance of directly multiplexed LC displays.
4. The potential for the development of the pocket and personal TV market.

Currently, panel sizes up to 14" diagonal have been reported. Pocket TV's of up to 6" diagonal are in production. An industry of TFT-LCD's is emerging.

*A program on TFT addressed electroluminescence (EL) panels was conducted in parallel with the TFT-LC effort at Westinghouse resulted in the demonstration of 6"x6" 20 lpi and 30 lpi TFT-El panels in 1973[22] and 1975[23] respectively.

15.3 DEVICE OPERATION

15.3.1 TFT-LC

As shown in Fig. 15.2, a color TFT-LC cell consists of a TFT matrix circuit glass plate and a color filter glass plate with the liquid crystal layer sandwiched in between. Each pixel element in the

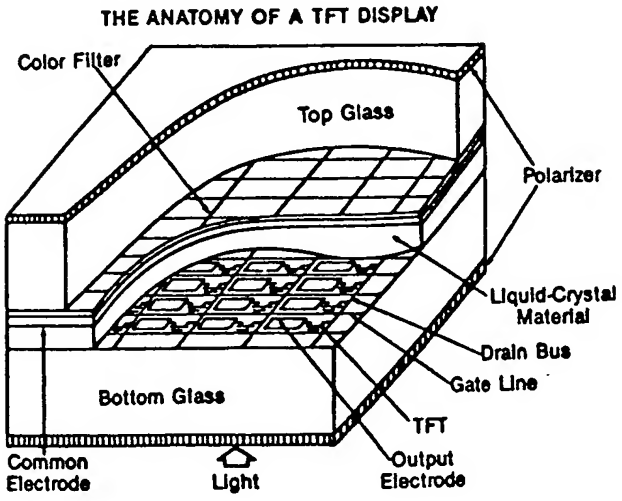


Figure 15.2 Cross sectional view of a TFT-LC cell[30]

display cell is defined by the row and column bus lines in the TFT matrix circuit. The electrical circuit diagram of each pixel element is shown in Fig. 15.3. Each pixel element has one TFT and a LC capacitor formed between the indium tin oxide (ITO) transparent output electrode on the TFT matrix circuit and the ITO back plane electrode on the color filter with the LC layer as the insulator. To operate the TFT-LC cell, an one-line-at-a-time addressing method is used. When a row (scan or gate line) is addressed, a positive pulse is applied to the line turning on all TFT's along the row. The TFT's act as switches transferring charges to LC capacitors from the respective columns (source or data lines). When other rows are addressed, a negative voltage is applied to the gate line turning OFF the TFT's along the line and holding the charges in the LC capacitors for one frame time until the line is addressed again. If the LC used in the cell is twisted nematic (TN), it is desirable to use AC voltage to drive the LC element. The polarity of the data voltage switches in alternate frames. An example of the

driving voltage waveforms of both the gate and the source lines is shown in Fig. 15.4[31].

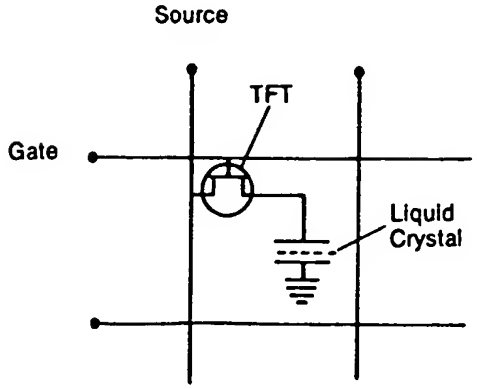


Figure 15.3 Electrical Circuit diagram of one pixel element

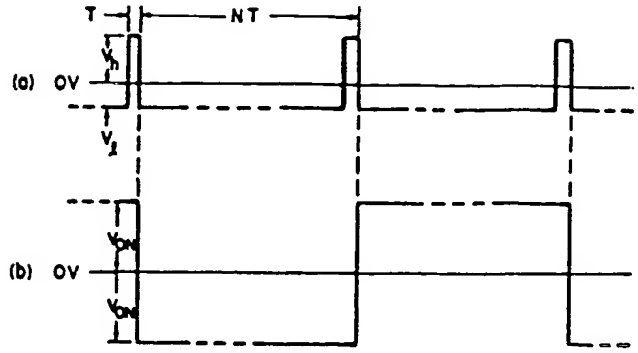


Figure 15.4 An example of the driving voltage waveforms of both the gate and source lines

The TFT device works like a MOSFET. The characteristics of a TFT generally can be represented by

$$I_{SD} = (W\mu Cg/L)V_{SD}\ (V_G - V_T - V_{SD}/2)$$

when $V_{SD} \leq (V_G - V_T)$,

$$I_{SD} = (W\mu Cg/2L)\ (V_G - V_T)^2$$

when $V_{SD} > (V_G - V_T)$,

where W is the width, L the length of the conducting channel of the TFT, μ the effective mobility of the semiconductor, Cg the gate capacitance per unit area, V_{SD} the source-drain voltage, V_g the gate voltage, V_T the threshold voltage of the TFT and I_{SD} the source-drain current.

The requirement on the characteristics of the TFT's during the ON periods is

$$I_{ON} > 2K_1 C_{LC} V_{ON}\ N/T$$

where I_{ON} is the ON current of the TFT, K_1 a constant, V_{ON} the ON voltage of the LC element, C_{LC} the capacitance of the LC element, N the number of addressed lines in the display and T the frame time. For a bi-level display such as an alphanumeric or graphic display, the requirement on the pixel voltage is not very tight since all voltage above the ON voltage of the LC element will be acceptable. K_1 can

be a value between 1-10 to allow for any nonuniformity in the TFT's in the panel and the fact that the ON current of the TFT is not constant during the charging of the pixel[31]. For a 6.25" x 6.25" panel with 1024x1024 pixel elements, I_{ON} should be greater than 1.09×10^{-6}A if we pick K_1 to be 5.

For a grey scale operation, the RC time constant is required to be at least one third of the charging period to obtain less than 5% error. K_1 should be larger than 10. In this case, I_{ON} should be greater than 2.18×10^{-6}A. During the OFF periods, the TFT's are turned off. The OFF currents of the TFT's should be low so the charges stored in the LC capacitors will not leak away to affect the appearance of the panel. For a bi-level panel, there are two separate conditions. For an OFF pixel, the voltage on the pixel should not increase to a level exceeding the threshold voltage of the LC material and turn the pixel partially ON. For an ON pixel, the voltage on the pixel should not drop below a voltage so the pixel appears partially ON or OFF. For a typical LC material, this ΔV should be smaller than 1.5V. The requirement on the OFF current of the TFT is

$$I_{OFF} < K_2 \, \Delta V \, C_{LC}/T$$

where K_2 is an engineering factor which allows for the uniformity variations of TFT characteristics in a TFT array and the temperature variations of the OFF currents of the TFT's. For a typical a-Si TFT, the OFF current can increase by a factor of 10 when the temperature is raised from 20°C to 70°C. Again using the 1024x1024 cell as an example, ΔV = 1.5V and K_2 = 0.1, I_{OFF} should be less than 3.28 pA.

For a grey-scale display ΔV should be less than one grey level, or 0.08V for a 16-level panel, I_{OFF} should be less than 0.175 pA.

Another path for the charges stored in the LC capacitor to leak away is through the RC relaxation of the LC material itself[32,33,34]. For a 5% error of the RMS voltage on the LC capacitor, the RC time constant of the LC material is required to be 10 times the frame time

of addressing. For a display with a 16ms frame time, the RC time constant should be longer than 160ms. When considering the requirements of elevated-temperature performance of the cell, the room temperature RC time constant should be over 1 sec. In order to reduce the severe requirements on the TFT OFF currents and the LC RC time constant, a storage capacitor can be added to each pixel element[18]. The storage capacitor can be either a general ground capacitor[35] or a capacitor formed between the ITO output electrode and the following scan line[28]. The trade-off of these storage capacitor designs is the increased fabrication complexity and reduced yield. For displays with moderate and low resolution (<200 lines per inch) the storage capacitor is desirable but maybe not required. For high resolution displays (>500 lines per inch), the storage capacitor is considered to be a necessity.

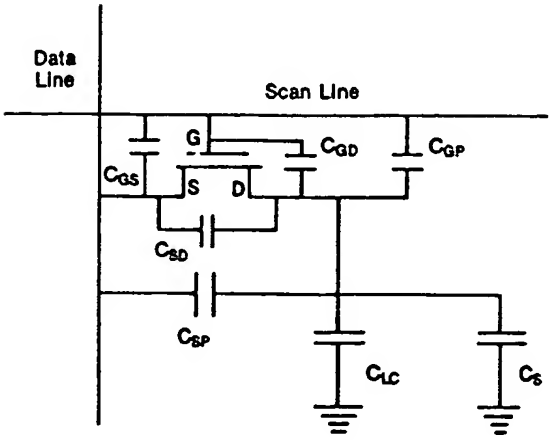


Figure 15.5 Parasitic capacitances in a TFT-LC circuit

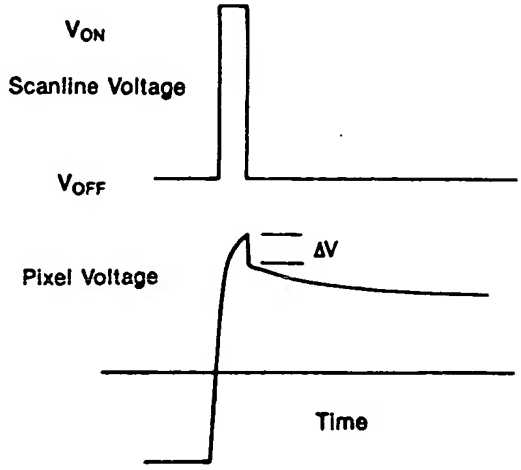


Figure 15.6 Voltage shift in the pixel voltage caused by the scan line voltage

In a TFT-LC circuit, there are many parasitic capacitances as shown in Fig. 15.5. C_{GD} is the capacitance in the TFT caused by the overlapping between the gate and drain electrodes. C_{GP} is the capacitance between the gate bus line and the ITO output electrode which is much smaller than C_{GD}. During the addressing of a line, when the scan line voltage is dropped from V_{ON} to V_{OFF} as shown in Fig. 15.6, a negative voltage shift $\Delta V=\Delta Vg\ C_{GD}/(C_{LC}+C_{GD})$ results

where $\Delta Vg=V_{ON}-V_{OFF}$. Because the geometry of the TFT array is not always uniform across the whole cell, and because C_{LC} is not a constant depending on the voltage applied to the LC element, this voltage shift can not be compensated by a simple voltage shift of the backplane electrode which will result in the problems of flicker and degradation of grey scale performance.

Here again, a TFT array with a storage capacitor in each pixel has the advantage of reduced voltage shift from coupling. Because of the anisotropy of the LC material, C_{LC} is not constant varying from a minimum of $C_{\perp}$ where no voltage is applied across the LC cell to a maximum of $C_{//}$ where the LC cell is fully turned ON. An example of a driving voltage compensation method[36] to achieve a symmetrical driving voltage across the LC cell is shown in Fig. 15.7. In this example, V_D is the data voltage applied to the data line, V_p the voltage to the LC pixel electrode, V_{com} the voltage of the common electrode, $dV_{p\perp}$ the voltage shift when the LC is OFF, $dV_{p//}$ the voltage shift when the LC is ON. The solid line is the pixel voltage before the voltage shift and the dotted line after the voltage shift. The data voltage $V_D = V_{sig-c} + V_{+amp}$ in one frame and $V_D = V_{sig-c} - V_{-amp}$ in the next frame. Typically, to obtain a symmetrical voltage across the pixel in all frames V_{+amp} is smaller than V_{-amp} and $V_{com} = V_{sig-c} - dV_{p\perp}$.

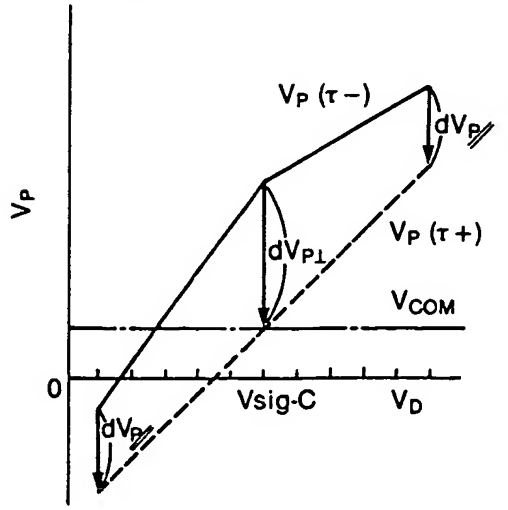


Figure 15.7 A voltage compensation method to obtain a symmetrical LC driving voltage[36]

Another major source of grey scale voltage distortion is through the capacitance coupling from the data voltages. The factor of the capacitor coupling is $(C_{SP}+C_{SD})/(C_{SP}+C_{SD}+C_{LC})$ where C_{SP} is the capacitance between the data line and the ITO output electrode and C_{SD} the source-drain capacitance of the TFT. For a 6V data voltage, this voltage shift could be in the order of 0.25V for a typical 164 lpi display design. Both neighboring data lines make contributions to this capacitance coupling effect. One example of this effect is a top to bottom brightness variation in the grey scale operation since the top of the cell sees the reverse-polarity data voltage for a shorter time than the bottom part of the cell. To compensate for this voltage shift, two methods have been proposed[37,38].

The first method[37] is the alternation of the data voltage polarity line by line and frame by frame. The second method[38] is to divide the addressing period of each line into two halves. In the first half, a normal data voltage V_i is applied. In the 2nd half, the TFT's in the row are turned off and a data complement voltage (V_m-V_i) is applied to the data line where V_m is a constant voltage.

As mentioned earlier, through the capacitance coupling between the gate and drain electrodes of a TFT and the gate line and the ITO electrode, the driving voltage across the LC cell is shifted by an amount which can be up to 4V in a typical 164 lpi TFT-LC cell. This LC voltage level shift can cause a net DC voltage on the LC element. When the driving voltage across an LC cell has a DC component, the transmission output of the cell has an asymmetry between the frame which has positive LC voltage and the next frame which has negative LC voltage. If the refresh rate of the cell is low, this can result in a visible flicker as shown in Fig. 15.8. One method to solve the problem is to increase the refresh rate to greater than 100 Hz so the flicker will not be visible[39]. Another method is using the line inversion technique mentioned earlier[37,40]. An example of the optical response using the line inversion technique is shown in Fig. 15.9[40].

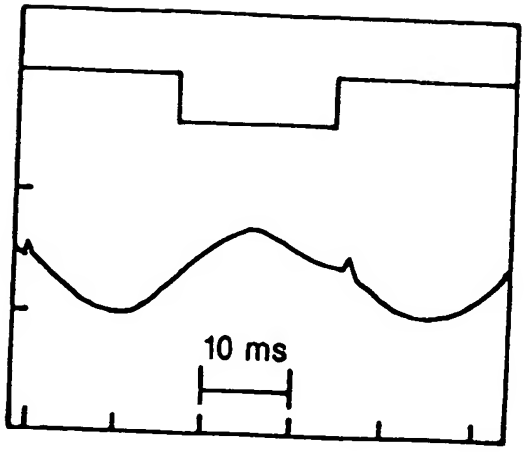


Figure 15.8 Flicker in a cell[40]. The upper trace is the driving voltage, the lower trace the optical response of a pixel

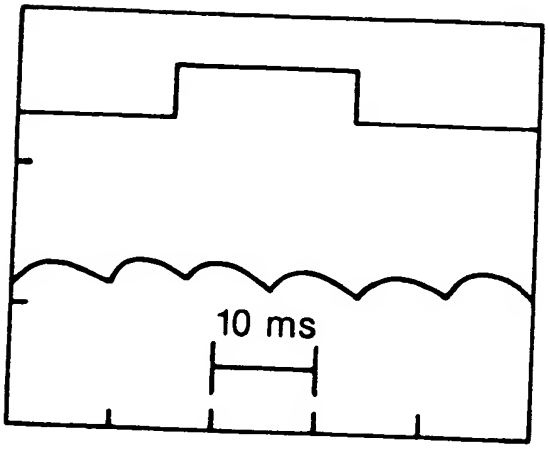


Figure 15.9 Optical response of a flicker-free pixel[40]

Many schemes to reduce line and pixel defects by improved circuit designs have been proposed. To eliminate crossover shorts between the gate and data lines which can cause 2 defective lines, a few designs[41,42,43] put the data and gate lines on separate glass substrates. One example is shown in Fig. 15.10[42]. To reduce display pixel defects, many designs with redundant bus lines[39] and redundant TFT's[44,45,46] have been proposed. An example[45] is shown in Fig. 15.11.

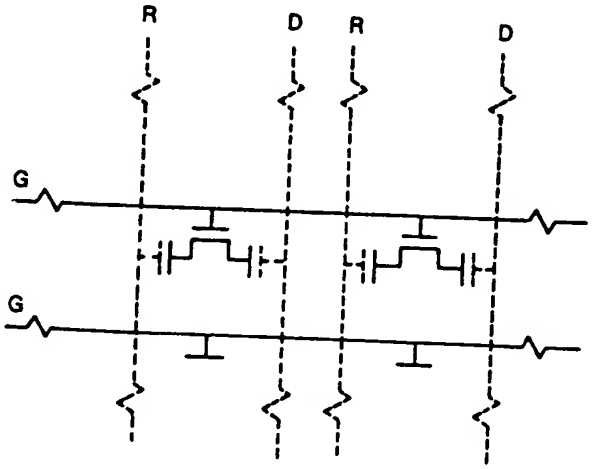


Figure 15.10 A TFT-LC design eliminating crossover[42]

In this design, each pixel has 2 individual TFT's connecting the pixel electrode to 2 neighboring data lines. If the data line is open, the correct data is supplied to the pixel electrode through the neighboring data line. If one TFT is defective or shorted, the TFT can be repaired or removed by laser trimming. This design has the further advantage of being able to electrically test all pixels without probing to detect defective pixels. To obtain the redundancy for TFT defects, some trade-offs on process complexity and output pad active area are required.

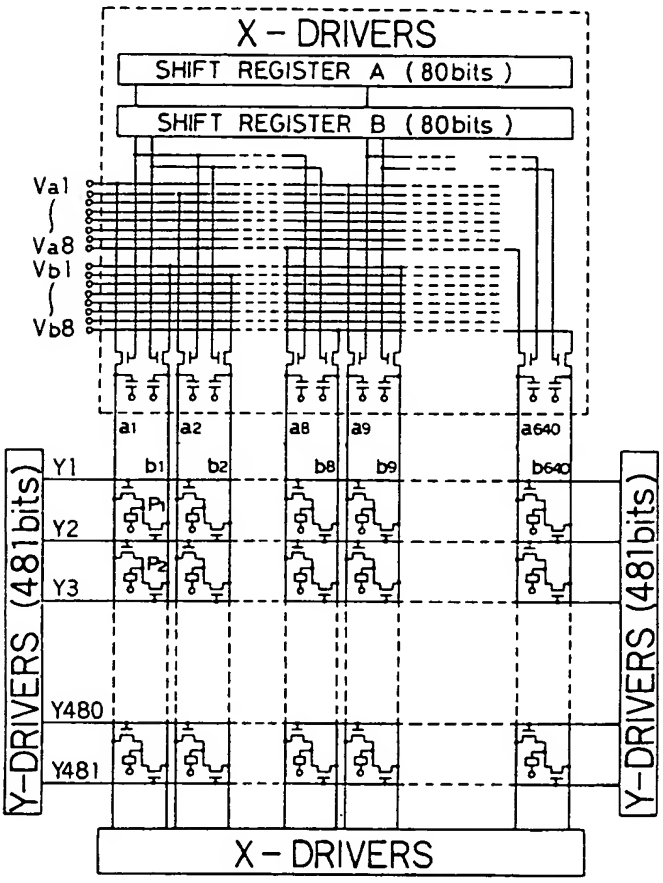


Figure 15.11 A TFT-LC circuit design with redundant TFT's in each pixel[45]

15.3.2 Diode LC Device

The structure of diode-LC devices is shown in Fig. 15.12. The ITO scanning lines are delineated on one piece of the glass while the data lines with diodes and ITO output electrodes are delineated on the other piece of the glass with the LC material sandwiched in between.

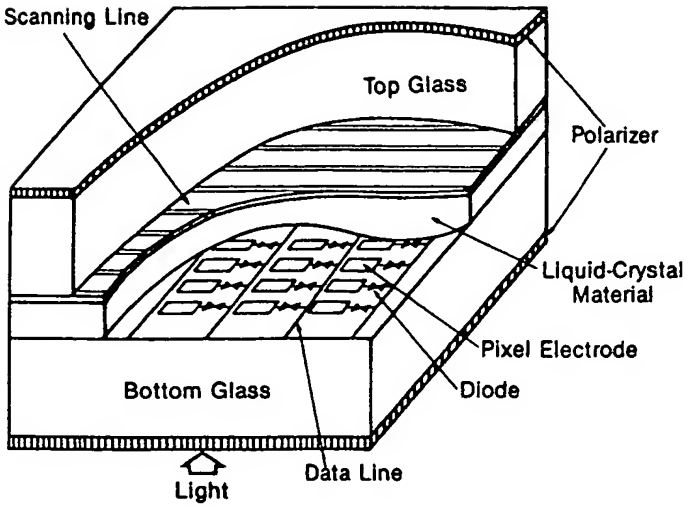


Figure 15.12 Structure of a diode-LC monochrome device

The schematic diagram[47] of one element of the cell and the addressing waveforms are shown in Fig. 15.13 and 15.14 respectively. The I-V characteristics of the diode are highly nonlinear and can be represented either by $I=KV\exp(BV^{1/2})$ for MIM or SiNx diodes or $I=A(V)^n$ for some other devices. When addressing a cell the addressed scanning line receives V_2, the rest of the lines 0 V in the odd frame. On the data line, the ON pixel has $-V_1$ and the OFF pixel $+V_1$. As a result, the voltage applied to an ON pixel is $V_{ON} = (V_2+V_1)-V_{td}$ where V_{td} is the threshold voltage of the diode. The requirements on the

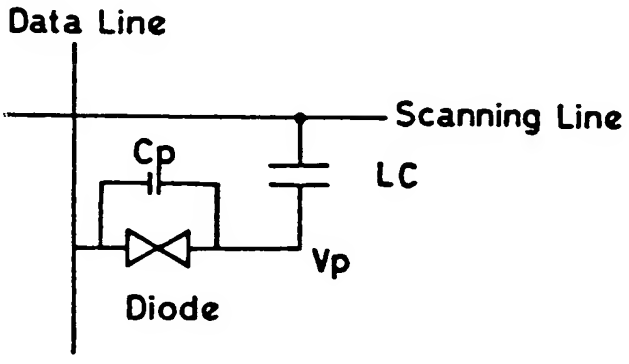


Figure 15.13 Elemental circuit of a diode LC device[47]

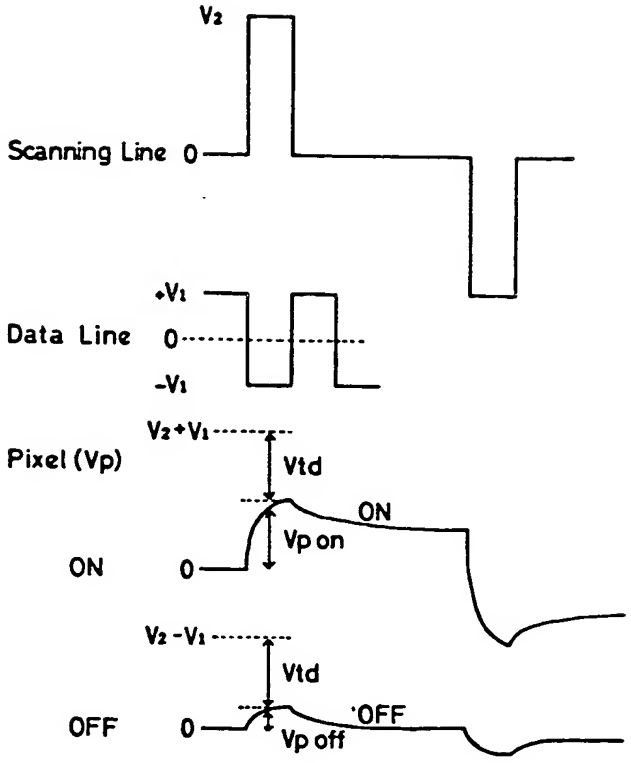


Figure 15.14 Addressing waveforms for a diode-LC device[47]

voltages are: $V_1 < V_{td}$, $V_{ON} > V_{SLC}$, $V_{OFF} \sim 0$ where V_{SLC} is the saturation voltage of the LC material. In the even frame, all voltages are inverted and an AC voltage is applied to the LC pixel. Since the diode threshold voltage V_{td} is a part of the pixel voltage, it is mandatory that the cell has a very uniform and stable V_{td} across the whole cell to obtain satisfactory operation. Another important requirement on the diode-LC device is that the parasitic capacitance of the diode C_p should be minimized ($C_p/C_{LC} < 10$ where C_{LC} is the LC pixel capacitance) to reduce the capacitance coupled voltage shift.

15.4 ARRAY FABRICATION

15.4.1 TFT Material

Three semiconductor materials, i.e. amorphous silicon (a-Si), polycrystalline silicon (poly-Si) and cadmium selenide (CdSe) have been widely investigated for the active matrix display application, each with

its unique fabrication processes. Each material has its pros and cons. CdSe TFT's have the longest history and have the required characteristics to perform in the matrix circuit and the peripheral driver circuits, but have not demonstrated a large-area high resolution color display. Due to the low-off-current and adquate-ON-current characteristics and its commonality in processing equipment with Si MOS device fabrication, a-Si TFT's have been the most popular and developed material. However, because of the capability of integrating the peripheral driving circuits with the matrix circuit on the same substrate, poly-Si TFT's are posing as the material of the future. Table 2 summarizes the comparison of the three TFT materials.

Table 15.2. A comparison between a-Si, poly-Si and CdSe TFT's

	a-Si	Poly-Si	CdSe
Mobility (cm^2/v-s)	0.3 - 1	10 - 100	25 - 150
Substrate	hard glass/sodalime	hard glass/quartz	hard glass/sodalime
Processing Temperature	<300°C	600 - 1000°C	<350°C
ON/OFF ratio	10^5 - 10^7	10^6	10^5 - 10^7
OFF Current	<1 pA	1- 10 pA	1 - 10 pA
Integrated drivers	Difficult	Product	Lab. Demonstrated
Largest size (diagonal)	14"	9.5"	9.5"
Most Pixels	1100 x 1440	480 x 960	400 x 640

15.4.2 TFT Structure

There have been two types of TFT structures commonly used in display applications as shown in Fig. 15.15(a) and (b). Fig. 15.15(a) is called an inverted staggered structure because the gate is at the bottom and the source-drain and the gate electrodes are on the opposite sides of the semiconductor. a-Si TFT arrays have used this structure

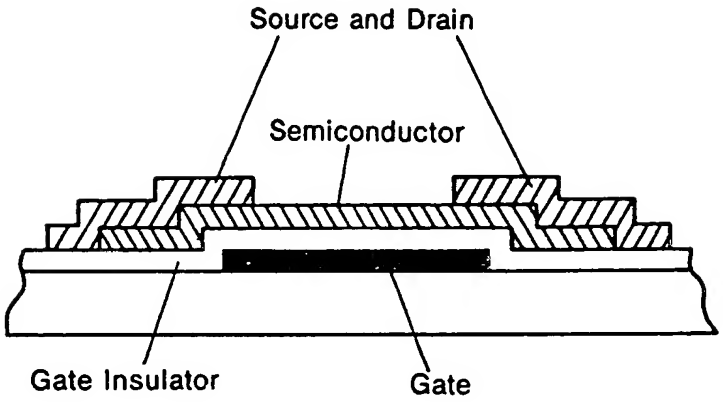


Figure 15.15(a)
Inverted staggered TFT

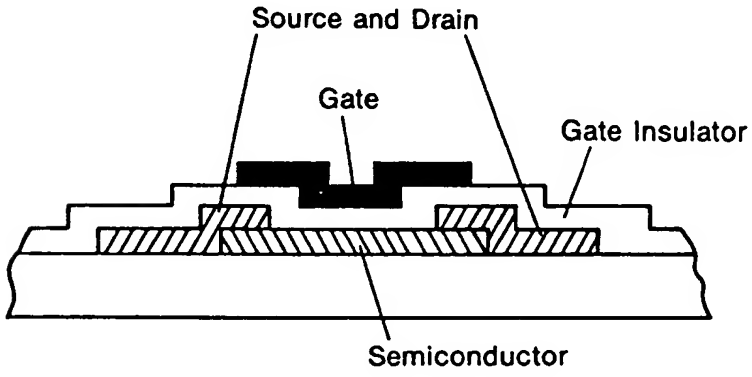


Figure 15.15(b)
Coplanar TFT

extensively. Fig. 15.15(b) is called a coplanar structure because the gate and the source-drain electrodes are on the same side of the semiconductor. This structure is popular with poly-Si TFT arrays. CdSe TFT arrays have used both structures.

15.4.3 a-Si TFT

The development of a-Si TFT's has benefited significantly from the advancement of a-Si solar cells in the 1970's. Extensive knowledge on the deposition techniques and electrical characteristics was accumulated during those years. The material was first applied to the TFT application in 1979[48] and has been extremely successful in TFT-LC applications primarily due to its high resistivity. The fabrication processes can be generally classified in two types, A and B. The sequence of the fabrication process for type A device is shown in Fig. 15.16[39]. The starting substrate is usually a low-sodium-content hard glass such as Corning 7059 glass. The gate material can be Ti, Ti-Mo, Cr, Ta, and

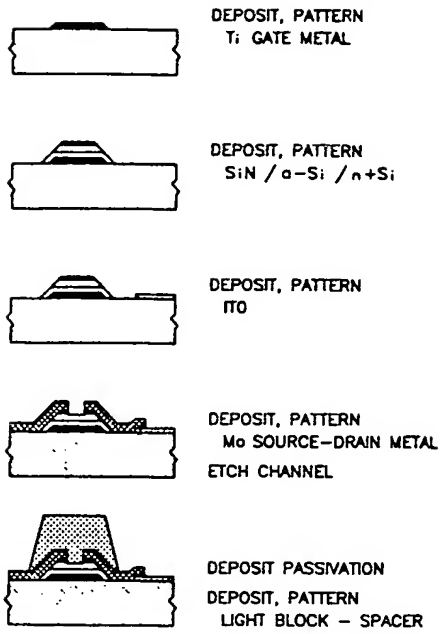


Figure 15.16 Fabrication process of a type A a-Si TFT array[39]

Mo-Ta, mostly deposited by DC magnetron sputtering. Ta and Mo-Ta gates have been widely used because the materials can be anodized yielding a pinhole-free gate insulator[49,4].

For the type A process, after the gate electrode delineation, a sandwich of SiNx, i-a-Si and n+ a-Si is deposited in one-vacuum-pump-down by the plasma enhanced chemical vapor deposition process (PECVD). The layers of n+ a-Si and i-a-Si are etched into islands for individual TFT's. After the delineations of S-D and ITO electrodes, the n+ a-Si layer is etched to form the conducting channels for the TFT's using the S-D electrode as the mask. A timed n+ a-Si or a differential n+ a-Si etch stopping at the intrinsic a-Si layer is used to etch away the n+ a-Si layer and leave behind the intrinsic a-Si layer. Finally, a thin SiNx layer is deposited on the array to passivate the devices.

For the type B process, a sandwich of SiNx, i-a-Si and SiNx is deposited in one-vacuum-pump-down using a PECVD. The top SiNx and i-a-Si layers are first etched into islands for individual TFT's, then the top SiNx layer is etched to expose the source-drain regions.

Following the etching, a thin layer of n+ a-Si and a source-drain metal are deposited in sequence in a PECVD and sputtering machine respectively. The source-drain (S-D) electrodes are patterned and etched. The typical S-D materials are Cr, Mo, Cr-Al and Ti. Finally, a thin ITO layer is deposited by sputtering and etched to form the LC output electrodes.

There are pros and cons comparing the two processes. The type B process requires 5 mask levels and needs careful cleaning of the interface before the deposition of the n+ a-Si layer to ensure obtaining good ohmic contacts for the TFT's. The type A process only requires 4 mask levels, however, because of the lack of efficient n+ a-Si etch stop, the thickness of the i-a-Si layer cannot be reduced to a few hundred angstroms to minimize the photoconductivity effect[50]. Also, in the type A device, the passivation SiNx layer is not deposited in the same pump down as the i-a-Si film, the OFF current and the photo current of the TFT in general are higher than type B devices[51]. The I-V characteristics of a typical a-Si TFT are shown in Fig. 15.17[51]. An

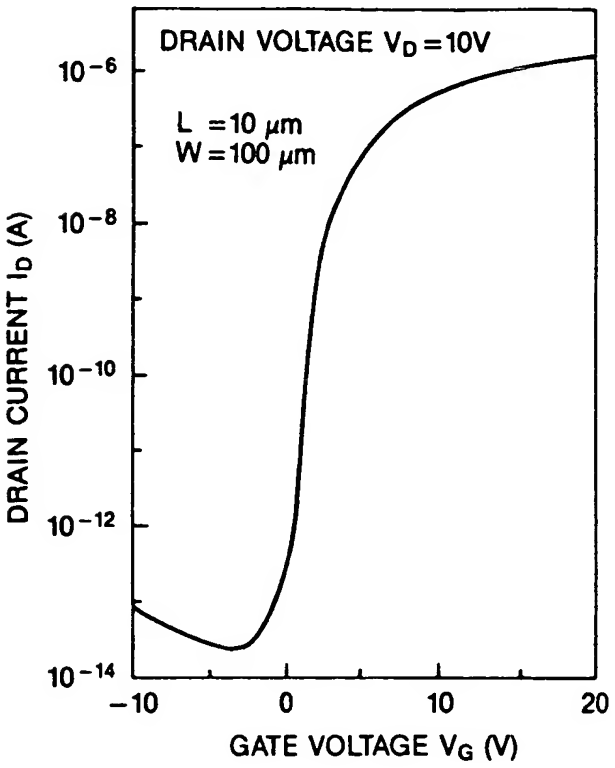


Figure 15.17 Characteristics of a typical a-Si TFT[51]

ON/OFF ratio greater than 10^6 and mobility between 0.3-1 $cm^2/v\text{-}s$ have been reported.

There are threshold voltage shifts in the TFT when DC biases are applied to the device. In general, as shown in Fig. 15.18, the threshold voltage is shifted to positive under a positive bias and to negative under a negative bias[52]. This is caused by charge injection into the gate insulator layer. The variable-range hopping model for the conduction in SiNx was proposed by Powell[53]. Suzuki et al. showed that the voltage shift corresponds to the summation of positive and negative biased period[54]. However, in a dynamic TFT-LC operation, due to the compensating forces of the alternating positive and negative voltages applied to the TFT stable operations can be obtained[55]. Fig. 15.19 shows the change of the ON current of an a-Si TFT vs. time in a practical TFT-LC operation at elevated temperatures[56]. An operation of more than 4000 hrs. at 80°C is assured if a limit of 4 volts for the TFT threshold voltage is assumed.

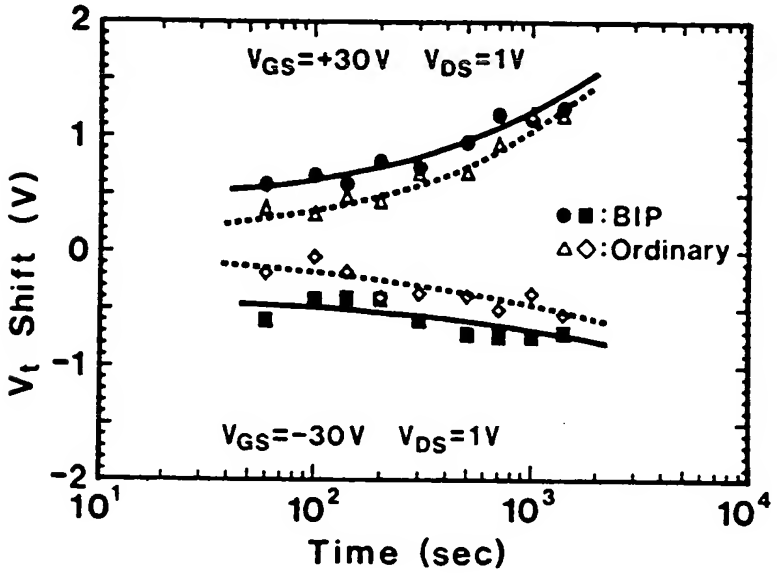


Figure 15.18 Threshold voltage shift of a-Si TFT's under DC biases[52] (BIP is a buried isolated pixel-electrode TFT)

15.4.4 Poly Si TFT

The fabrication processes of poly-Si TFT's are similar to the MOS technology. Poly-Si films are typically deposited by the low-pressure

CVD (LPCVD) process at around 600°C. The starting substrate is either quartz[57] or hard glass[58] depending on whether a thermally-grown oxide or a deposited low-temperature oxide is used as the gate oxide.

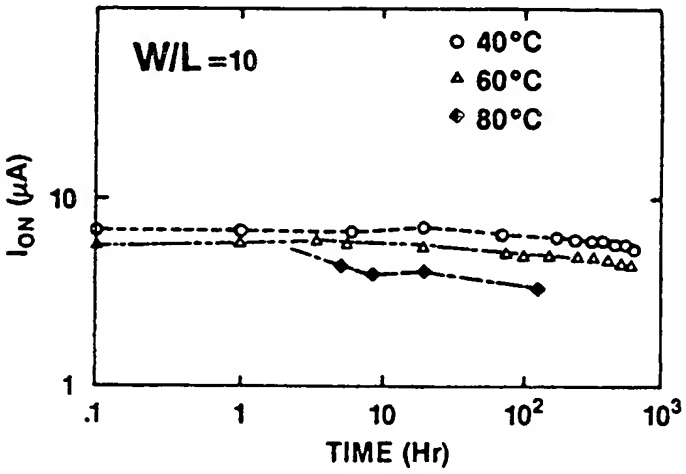


Figure 15.19 ON current change of an a-Si TFT vs time in a TFT-LC operation at elevated temperatures[56]

An example of the poly-Si TFT fabrication process is shown in Fig. 15.20[58,59]. First a 1500Å phosphorous doped poly-Si layer is deposited on a hard glass substrate and then etched as the source-drain electrodes. Then a very thin layer (typically 250Å) of undoped poly-Si film is deposited by a LPCVD system at 600°C and etched. An ITO film is then sputtered and etched into data lines and output electrodes. The gate insulator is 1500Å-thick SiO_2 deposited by a thermal CVD machine. Finally the Cr gate electrodes are sputtered and delineated. For the high-temperature poly-Si TFT, the gate insulator is thermally grown at around 1000°C and the S-D doping is accomplished by ion implantation.

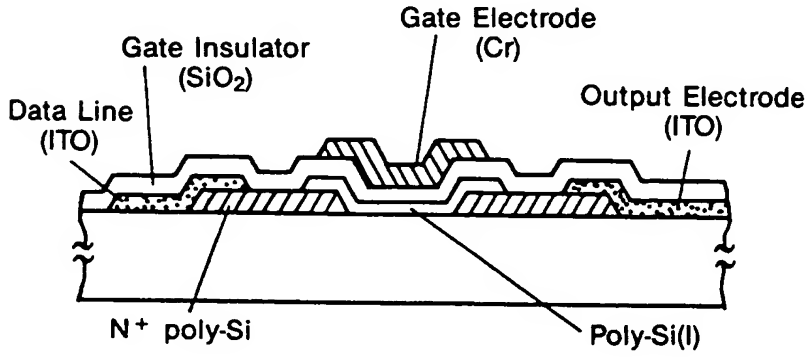


Figure 15.20 A poly-Si TFT fabrication process[58]

Self-aligned-gate processes have the advantage of minimized gate to drain electrode overlapping. Fig. 15.21 shows an example of a self-aligned-gate process[60]. First, a poly-Si layer is deposited and

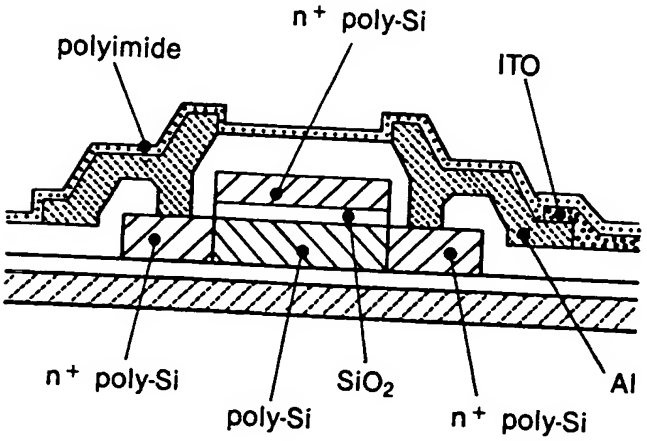


Figure 15.21 A self-aligned-gate poly-Si TFT fabrication process[60]

patterned into islands. Then a layer of SiO_2 and a layer of poly-Si are deposited sequentially and etched, exposing the two ends of the poly-Si islands. The exposed poly-Si material is then doped by ion implantation. The top poly-Si serves as the gate electrode. The top poly-Si along with the SiO_2 layer also act as a mask defining the source drain regions of the TFT (self aligning). After depositing another layer of SiO_2 and via-hole etching, Al is deposited and delineated to serve as source-drain electrodes. Finally, ITO is sputter deposited and etched as output electrodes.

Another promising poly-Si process is to convert a-Si films into poly-Si films by laser annealing[61]. This way, both poly-Si and a-Si TFT's can be processed on the same substrate. The a-Si TFT's can be used for the matrix array and poly-Si TFT's for the driver circuits.

The characteristics of a typical poly-Si TFT fabricated by the low-temperature process are shown in Fig. 15.22 [58]. The conducting channel width to length ratio is $10\mu m/10\mu m$ and the electron mobility is about 10 $cm^2/v\text{-}s$. Electron mobilities in poly-Si TFT's up to 100 $cm^2/v\text{-}s$ have been reported.

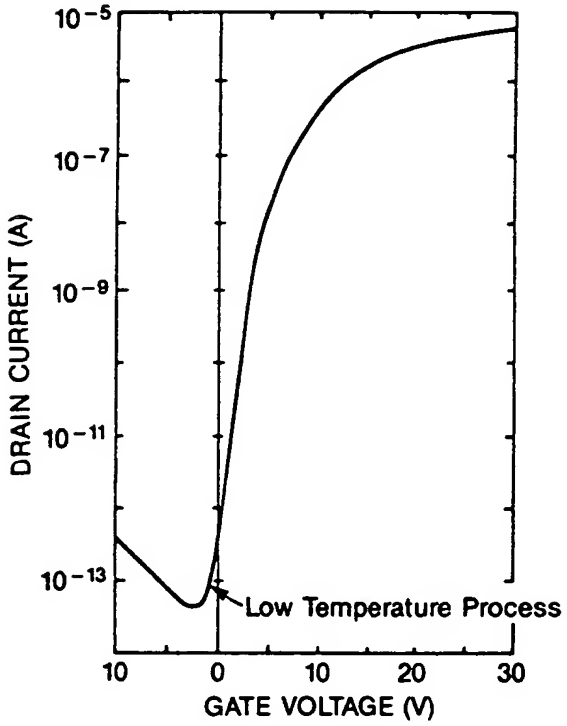


Figure 15.22 Characteristics of a poly-Si TFT[58]

One of the major advantages of poly-Si TFT's is the application to integrated row-column driver circuits[60] which can significantly reduce the required display interconnections and increase the compactness and reliability of the display. For an interlaced TV operation, the row drivers should operate at 16 KHZ. The operation can be obtained by a semiconductor with a mobility of about 0.5 $cm^2/v\text{-}s$. Therefore, a-Si, poly-Si and CdSe all can be used for this application. For column drivers, the operating frequency has to be greater than 8 MHZ for mono and 23 MHZ for color panels. A minimum mobility of 10 $cm^2/v\text{-}s$ is required which excludes a-Si.

Fig. 15.23 shows the operating frequency of typical poly-Si shift registers[62]. For a CMOS shift register with a 20-volt supply voltage, the maximum operation frequency is 1.25 MHZ. In order to obtain the required operating frequency, matrix switches[63] are used to divide the data lines into parallel blocks (such as 8 or 9). So far, demonstrated TFT-LC devices with integrated drivers have been limited to relatively small sizes (3" diagonal, 640x480)[64]. In the case of large-area

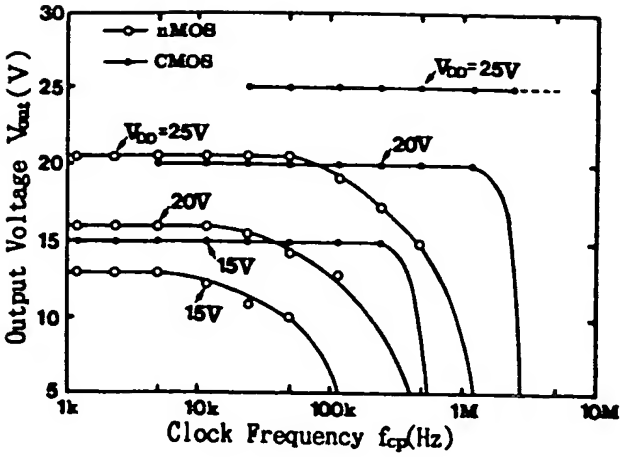


Figure 15.23 Output voltage vs. clock frequency characteristics of Poly-Si shift registers[62]

displays where the cost of the display is high, the integrated-driver approach may not be economical[65]. The size of the largest poly-Si cell has been 9.5", 480x960 pixels[59].

15.4.5 CdSe TFT

CdSe has been applied to AM displays since the 1970's[19,66]. It has the advantages of being a low-temperature processing material and having a relatively high mobility of up to 100 $cm^2/v\text{-}s$. In the early days, CdSe devices were fabricated by using shadow masks[26] which had the limitations of low resolution (<50 lines per inch) and particle contamination. The largest reported CdSe TFT-LC cell was fabricated by an all-photolith process[29] on a 10"x7" glass with a resolution of 80 lpi and a pixel count of 640x400 elements (Litton is reported to be working on a 6"x8", 960x1280 cell). The flow chart of the process is shown in Fig. 15.24. The TFT's had the inverted-staggered structure. All layers were delineated by lift-off processes except the ITO layer, which was patterned by etching. The Ni gate electrodes, ITO output pads, and the Al_2O_3 gate insulator were deposited by sputtering. The CdSe and In-Au source-drain electrodes were deposited on room-temperature substrates in a vacuum system which had a load lock and resistance-heated and electron-beam sources. Typical TFT's had ON currents of about 1μA at 20Vg and $10V_{SD}$ and OFF currents of about 100pA at $0V_g$ and $10V_{SD}$.

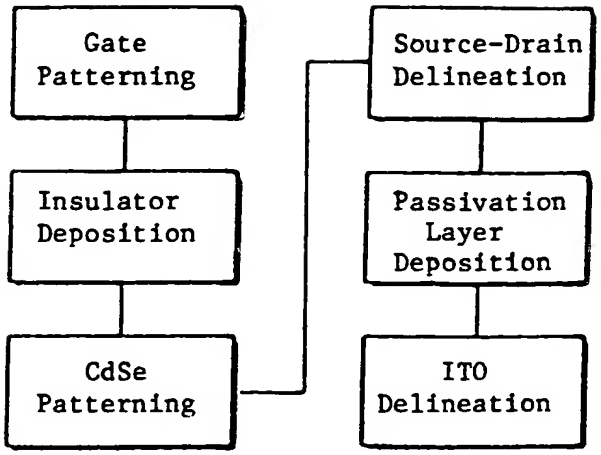


Figure 15.24 Flow chart of an all-photolith CdSe TFT fabrication process[29]

The other reported CdSe fabrication process used the anodized Ta_2O_5 [67] as the gate oxide and demonstrated the operation of a 12,288-pixel 128x96 LC cell. In the report, TFT's had ON currents of 1.4 μA at $20V_g$ and $10V_{SD}$ and OFF currents of <1pA at $0V_g$ and $10V_{SD}$. The mobility of the CdSe film was 100 $cm^2/v\text{-}s$.

One of the potential advantages of the CdSe TFT approach is the integration of row and column driver circuits with the matrix circuits. Some results have been reported[68],[69].

15.4.6 Diode

The fabrication processes of the a-Si diode arrays are similar to a-Si TFT arrays which require 5-6 masking levels and the depositions and delineations of metals, ITO and a-Si layers. Fig. 15.25 shows the fabrication process of a MIM diode with the anodized Ta_2O_5 as the insulator[70]. First, a Ta film is sputter deposited on the substrate coated with a layer of thermally grown Ta_2O_5 film. Then the substrate is coated with a layer of 5000A-thick polyimide film which is patterned into data lines and diodes. Using the polyimide film as a mask, the Ta film is dry etched into data lines with tapered edge profiles. Then the exposed edges of the Ta films are anodized in citric acid with 20-30V bias to obtain an oxide layer with a thickness of about

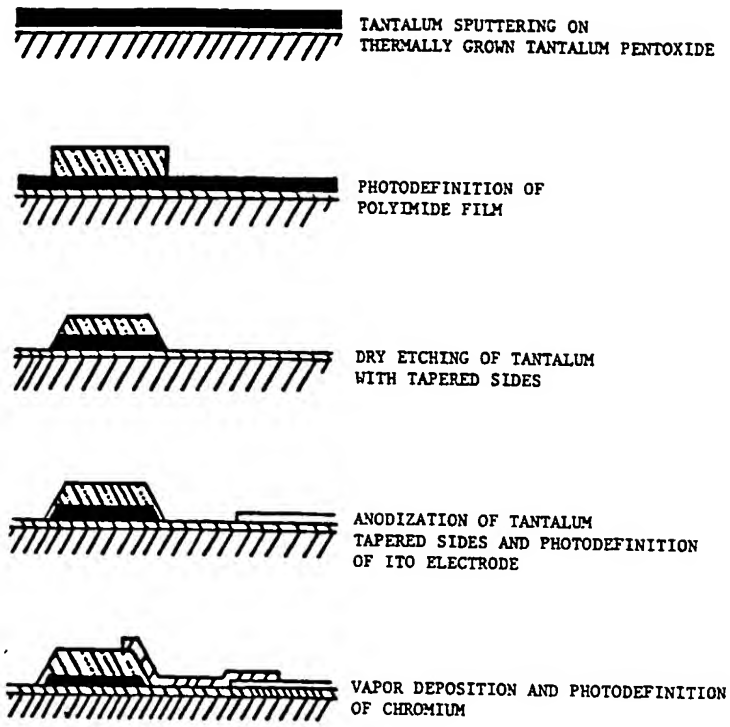


Figure 15.25 Fabrication process of a Ta_2O_5 MIM diode[70]

500Å. Following the delineation of an ITO layer as the LC output electrode, a Cr layer is used to produce a symmetrical contact for the diode.

This process has the advantage of simplicity with only 3 photomasking steps. However, the problems with large parasitic capacitance and gradual I-V nonlinearity may prevent this device to achieve the large-area high quality grey scale performance.

15.5 CELL ASSEMBLY

The cross-sectional view of a TFT-LC cell is shown in Fig. 15.2. The cell consists of primarily two pieces of glass, i.e., one TFT array and one color filter with LC sandwiched in between. A typical fabrication process flow is shown in Fig. 15.26. First, both pieces of glass are coated with a thin layer of polyimide with a thickness ranging from a few hundreds to one thousand angstroms. Then both plates are rubbed in prearranged directions by a rubbing wheel to obtain LC molecule

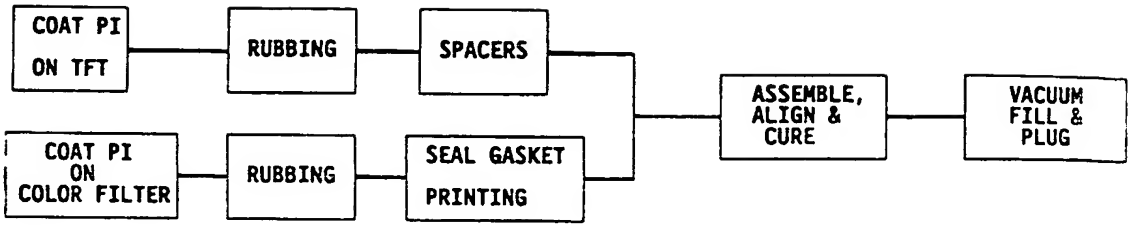


Figure 15.26 Process flow of the cell assembly process

alignments. Next, a narrow strip of Epoxy is either dispensed or printed on the boarders of the color filter glass to form a ring with a narrow opening. To obtain the proper spacing between the two glass plates, which ranges between 4 to 10 μm, fiber glass spacer rods or spacer beads are dispensed randomly and uniformly on the TFT substrate. Another technique is by delineating a dyed polyimide post on each TFT which not only maintains the proper spacing, but also serves a light blocking function. The color filter and the TFT array are assembled together with the pixels in the TFT array properly aligned with the pixels in the color filter. The two plates are also arranged to have the surface rubbing directions to be 90^0 relative to each other so the LC molecules will make a 90^0 twist going from one plate to the other. After pressing and curing, the assembly is vacuum filled with LC and plugged by a quick-setting Epoxy.

Many types of color filters have been reported in the literature for the color LC display applications which include dyed gelatin[71], dyed polyimide[72], electro deposition from a dispersion of polymer, dispersing agent and pigments[73,74], and colored inks[74]. Among these, the most widely used type is the dyed gelatin color filter. A typical fabrication process[71] is as shown in Fig. 15.27. The gelatin layer has a thickness between 1-2 μm and is dyed three times separately to obtain the three colors. To enhance the contrast of the cell, a black matrix between dyed pixels can be included. This black matrix is obtained either by using black dyed gelatin[35] or by fabricating the color filter on a substrate with a matrix of black chrome film[75].

Typical transmissive spectra of a dyed gelatin color filter are shown in Fig. 15.28[76]. There are four common color pixel arrangements in a color filter as shown in Fig. 15.29[77]. Arrangement 3 is the most popular one for TV applications, while arrangement 4 is considered to be

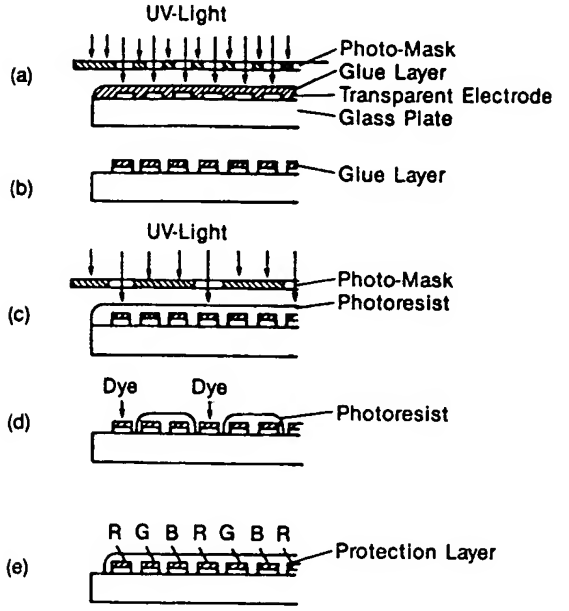


Figure 15.27 A gelatin color filter fabrication process[71]

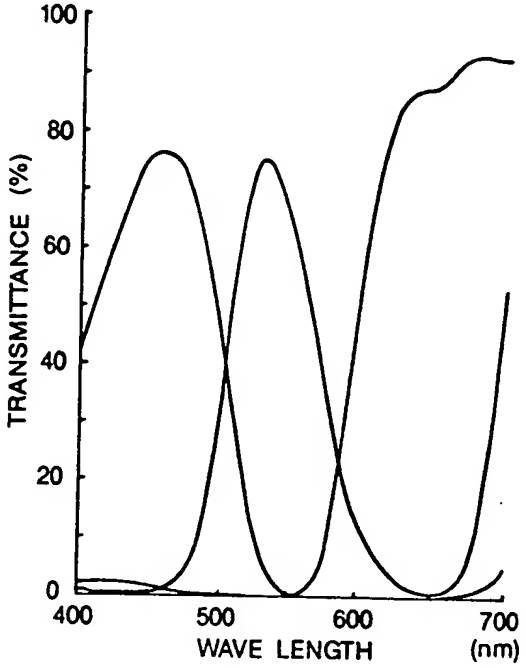


Figure 15.28 Transmissive spectra of a dyed gelatin color filter[76]

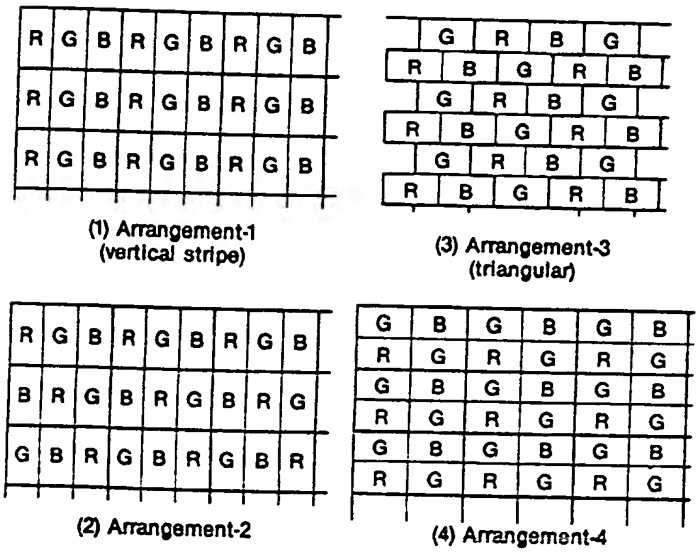


Figure 15.29 Color pixel arrangements in a color filter[77]

suitable for graphic and alphanumeric applications. Another variation of the arrangement 4 color filter is replacing one of the green pixels with a white pixel to increase the light transmission of the ON state.

Despite early attempts to utilize guest-host LC materials[75] to achieve wider viewing angle, now almost all TFT-LC displays use the TN effect, primarily due to bulk resistivity considerations. In order to achieve the charge storage effect in each pixel in a refresh time frame, it is essential to have, in addition to low TFT OFF current, high resistance in each LC pixel[34,78]. The resistivity of the LC material needs to be greater than 10^{11} ohm-cm at the operating temperature to achieve satisfactory operation. For a cell meeting military specifications, the operating temperature is required to be greater than 70°C. The resistivity of the LC material needs to be greater than 10^{12} ohm-cm in room temperature. The resistivity of the LC material in a cell is also affected by the alignment polyimide material, the buffing material, the cleaning procedure after buffing and the sealing Epoxy. Great care in handling all these areas needs to be exercised to obtain the optimized cell performance.

15.6 OPTICAL PERFORMANCE

Presently all AM LC devices use the TN effect primarily because of the high bulk resistivity requirement of the TFT-LC circuit. The front and back polarizers of the TN cell can be arranged to be either parallel or perpendicular to each other to obtain either the normally black or normally white effect. The electrooptical measurements of the LC cells with the two arrangements are shown in Fig. 15.30. Usually due to some charge loss in the LC capacitor in an addressing period, TFT-LC cells require slightly higher data voltages to maintain the same transmissivity as a direct-drive LC cell. Also, cross-polarized cells require higher data voltages than parallel-polarized cells to obtain the saturated dark OFF state. Color AM LC devices have been exclusively in the transmissive mode. To achieve the desired efficiency and brightness

in a color LC cell, RGB fluorescent lamps should be used as the back lighting. The spectral distribution of such a lamp is shown in Fig. 15.31[79].

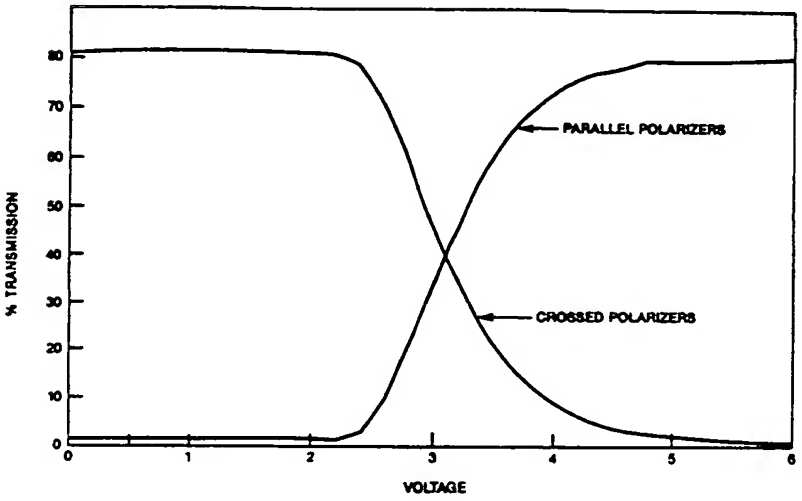


Figure 15.30 Transmittance vs. driving voltage of TN LC cells with parallel and crossed polarizers

In this lamp, specially mixed phosphors are used to generate light emission with spectra matched with the peak transmissions of the color filters to maximize the transmission efficiency [5,79,80]. There are both advantages and disadvantages comparing parallel vs.

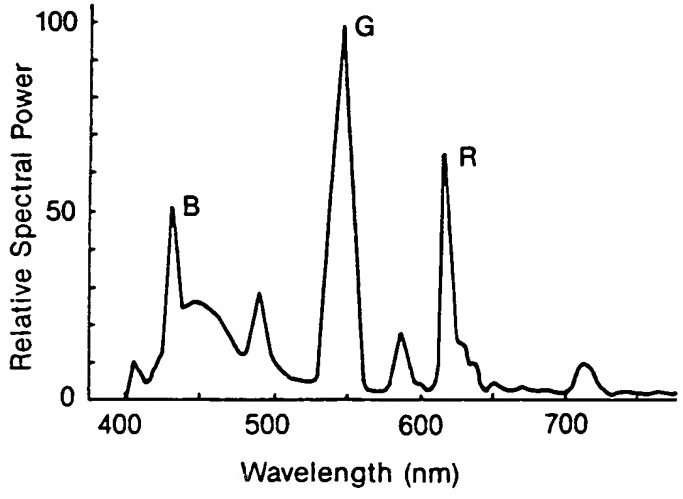


Figure 15.31 Spectral distribution of a RGB lamp[79]

crossed polarizers. Fig. 15.32(a) and (b)[81] show the contrast ratios vs. Δnd for cells with parallel and crossed polarizers respectively where Δn is the birefringence of the LC material and d the cell thickness in μm. As shown in the figures, the contrast of parallel-polarized cells has more stronger dependence on Δnd than cross-polarized cells. Parallel-polarized cells require critical cell thickness control to obtain a very dark OFF state and an acceptable OFF state uniformity. Parallel-polarized cells also have more severe degradation of the OFF state at elevated temperatures when Δn is reduced.

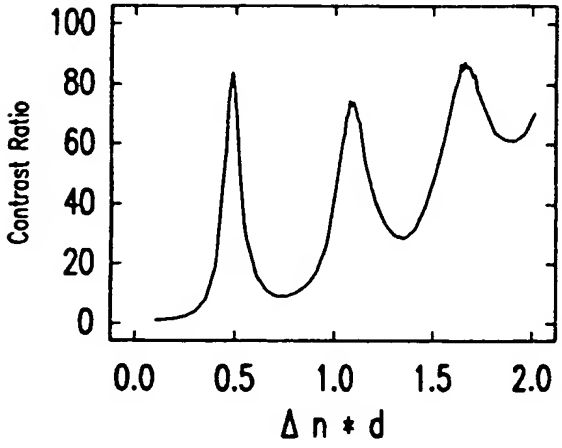


Figure 15.32(a) Contrast ratios vs. Δnd for cells with parallel polarizers[81]

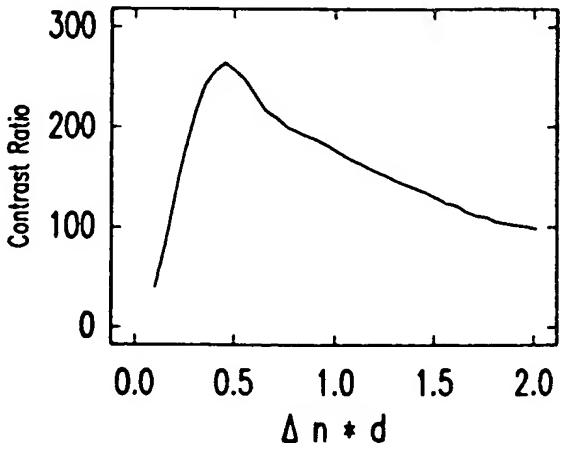


Figure 15.32(b) Contrast ratios vs. Δnd for cells with crossed polarizers[81]

Because of the anisotropy of the polarizers and the LC material, the appearance of LC cells is angle dependent. Fig. 15.33, and 15.34 show the transmittance vs. driving voltage curves for different viewing angles for cells with parallel and crossed polarizers respectively[82]. There are significant top to bottom brightness variations for both parallel- and crossed-polarizer modes. The left to right brightness variation is less for the crossed-polarizer mode than for the parallel-polarizer mode.

There are some color shifts of the display vs. viewing angles also. The comparison of the black colors of the OFF states of the

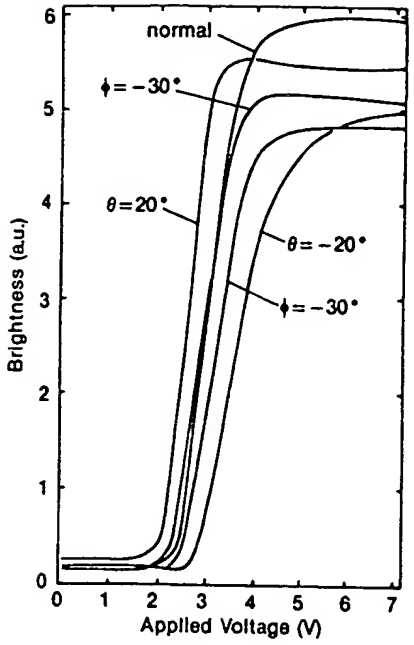


Figure 15.33 Cell brightness vs. driving voltage for different viewing angles for a cell with parallel polarizers. θ is for top to bottom and ϕ is for left to right viewing angles[82]

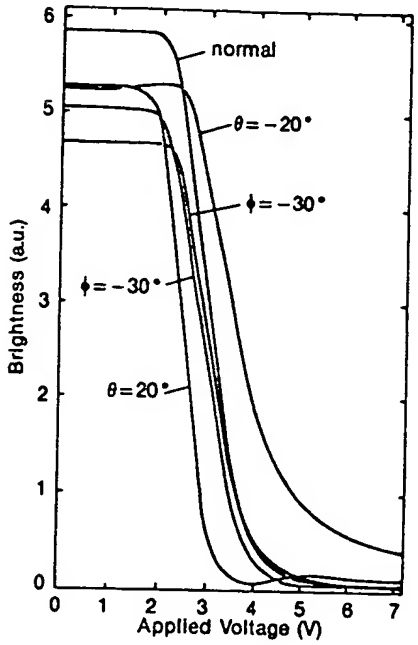


Figure 15.34 Cell brightness vs. driving voltage for different viewing angles for a cell with crossed polarizers. θ is for top to bottom and ϕ is for left to right viewing angles[82]

parallel- and crossed-polarizer cells is shown in Fig. 15.35[83]. As indicated in this figure, there are more color shifts of the OFF state in the parallel-polarizer mode than the crossed-polarizer mode.

Two reported display panels are used here to exemplify the TFT-LC cell performance. One is a Sharp panel using the crossed-polarizer arrangement[83], the other a Matsushita panel using the parallel-polarizer arrangement[35]. The contrast ratio dependence of viewing angles of the Sharp panel is shown in Fig. 15.36. A contrast ratio over 100:1 was obtained.

The color coordinates of the cell back illuminated by a fluorescent lamp is shown in Fig. 15.37. The contrast ratio dependence of viewing angle and the color coordinates of the Matsushita cell are shown in Fig. 15.38 and 15.39 respectively. A contrast ratio of over 50:1 was reported.

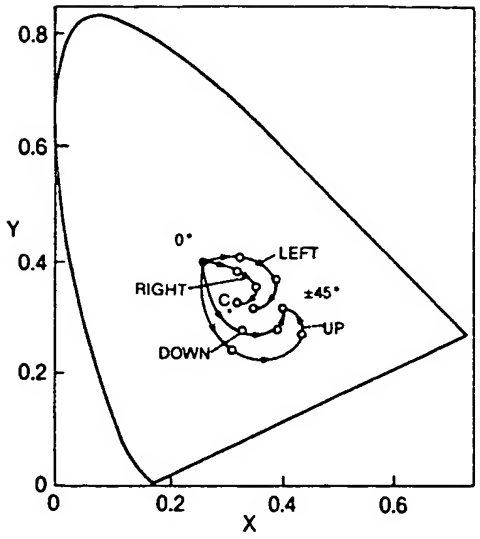


Figure 15.35(a)

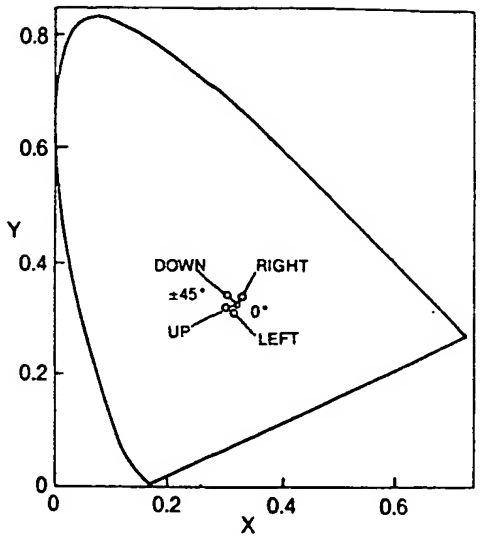
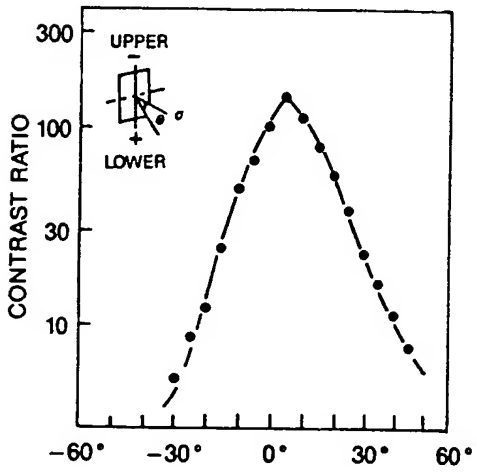


Figure 15.35(b)

The OFF-state color variations vs viewing angles of TFT-LC cells on the CIE chromaticity diagrams with (a) parallel (b) crossed polarizers[83]



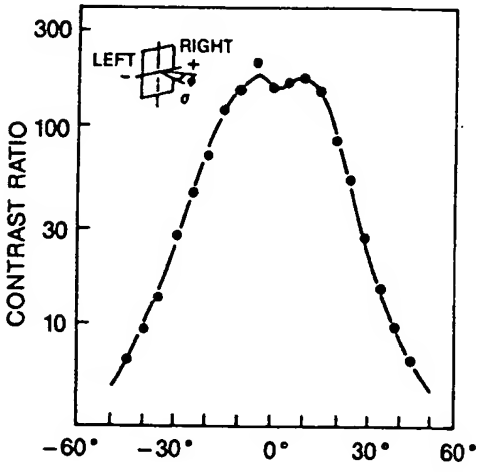


Figure 15.36 Viewing angle dependence of contrast ratio for a crossed-polarizer TFT-LC cell[83]

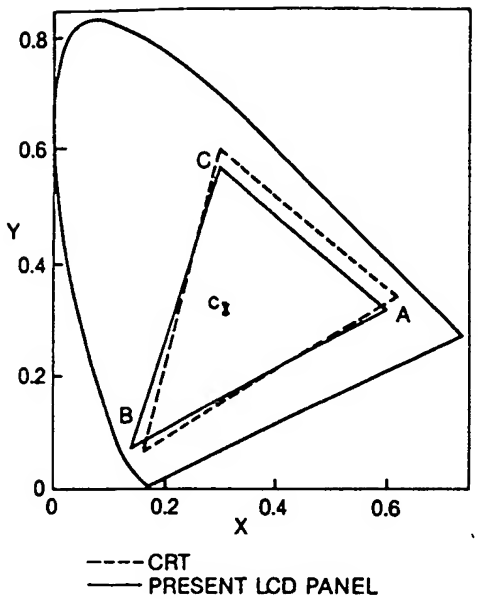


Figure 15.37 CIE color coordinates of a crossed-polarizer TFT-LC cell back-illuminated by fluorescent lamps[83]

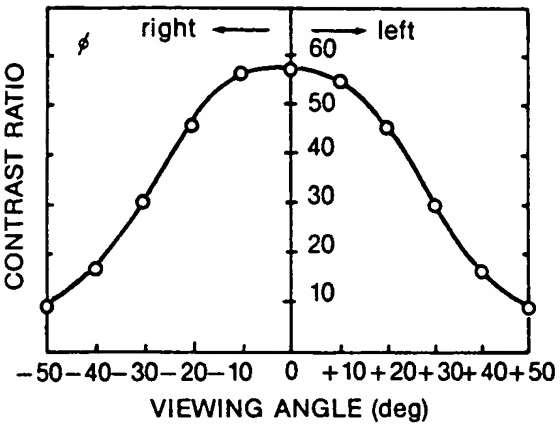


Figure 15.38(a) Viewing angle dependence of contrast ratio for a parallel-polarizer TFT-LC cell[35]

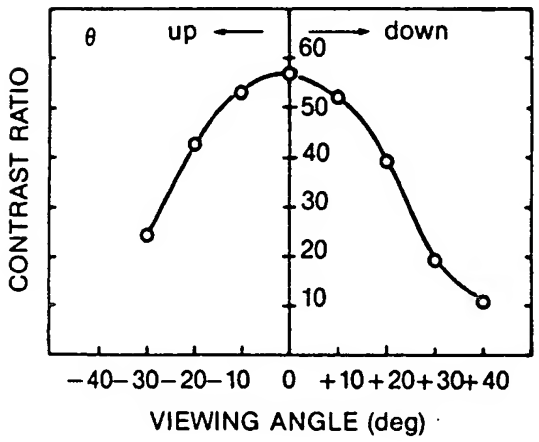


Figure 15.38(b) Viewing angle dependence of contrast ratio for a parallel-polarizer TFT-LC cell[35]

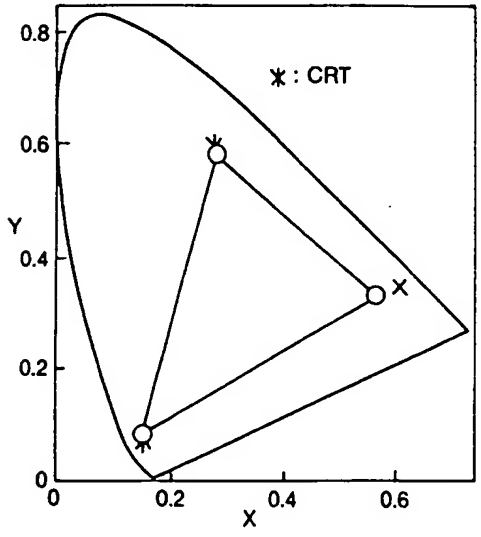


Figure 15.39 CIE color coordinates of a parallel-polarizer TFT-LC cell[35]

Another example of the cell performance optimization through Δnd adjustment is shown in Fig. 15.40 where a cell with Δnd=1.49μm yielded a black OFF state and the least viewing angle variation[4]. Another important feature of the TFT-LC display is the viewability under very bright ambient conditions. A contrast ratio of greater than 4:1 under 10,000 fc of diffused ambient illumination when viewed normal to the cell has been reported[5]. The typical response time of a TFT-LC cell is between 20-40 ms.

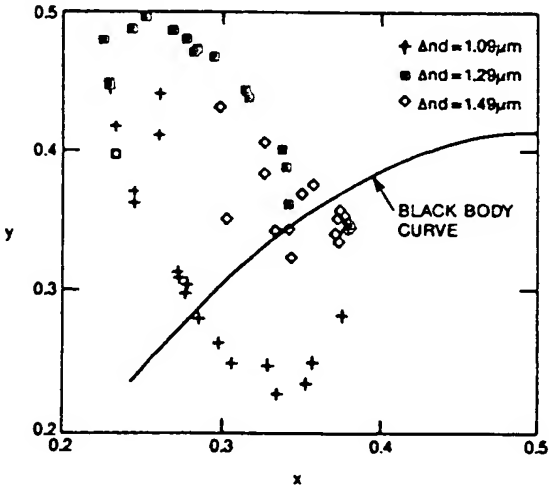


Figure 15.40 Background color change due to change in cell retardation[4]

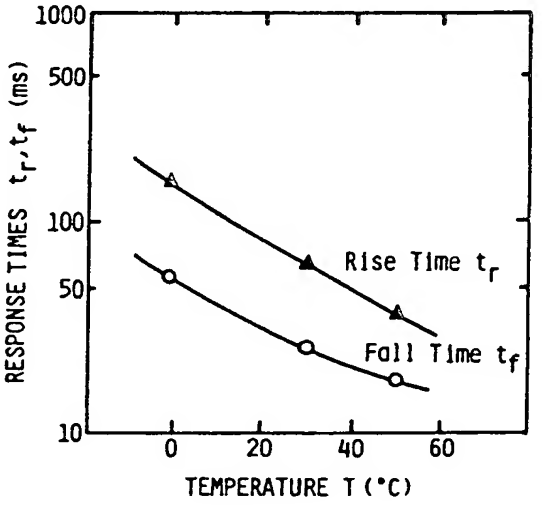


Figure 15.41 Temperature dependence of the response time of an LC cell[84]

The performance of a TFT-LC cell is strongly affected by temperature. Fig. 15.41 shows the temperature dependence of the response times of an LC cell[84]. The cell has response times in the 1-2-second range at -40°C and needs a heater to obtain satisfactory operation at cold temperatures. The ON and OFF currents of the TFT[85] and the resistivity, the threshold voltage (decreasing by about 0.1 v per 10°C increase) and the birefringence (decreasing by about 0.003 per 10°C increase) of the LC material all change significantly at elevated temperatures which cause strong temperature dependence of important cell characteristics such as contrast ratio, viewing angle

and color gamut. Nevertheless, operation of TFT-LC cells between -40°C to 85°C has been demonstrated.

Fig. 15.42-44 show the performance of a few representative TFT-LC cells.

15.7 STATUS AND FUTURE TREND

In the last few years, the development of TFT-LC devices has been progressing at an explosive pace. The sales of TFT-LC devices are predicted to be over 1 billion dollars in the early 1990's[87]. Presently, world-wide there are more than 25 companies actively engaging in AM LCD activities. Table 3 shows a list of recently reported AM LC devices[34]. The displays are getting larger and denser every year. The largest display size has been expanded to 14" diagonal[3,4], the highest resolution to 400 lines per inch[88] and the most display pixels to 1.54 million[4].

Currently, TFT-LC devices have been applied to direct-view TV, projection TV, computer displays, instrumentation displays and military avionic displays. In almost all of these applications, the color AM LC devices have adequate color gamut, grey scale capability, response time, resolution, power consumption and high-ambient viewability to compete with CRT's. The areas where improvements are required are manufacturing cost, large-size availability and viewing angle.

At this moment, the price of AM LC device is about more than 5 times higher than an equivalent-size CRT. This price differential needs to be reduced significantly to make AM LC devices widely acceptable to customers. The cost can be lowered through throughput improvements of the projection photoresist alignment exposing system and the PECVD deposition machine for the AM fabrication. The developments of integrating driver circuits on the same substrate as the AM by poly-Si devices or using the chip-on-glass technology can

reduce the driver electronics cost.

The fabrication of large-area devices up to 40" diagonal is primarily limited by the availability of processing equipment. Beside the requirement for development of some high conductivity metal layers for the row and column lines there should be no fundamental limitation for the expansion into large area. Another approach to large-area displays is by projection which can use small size displays. Several very impressive projection displays have already been demonstrated[88,89].

Table 15.3. Current TFT-LC Activities

COMPANY	DIAGONAL SIZE (in.)	RESOLUTION	ACTIVE MATERIAL	DISPLAY TYPE	STATUS
CNET	4.2	288X320	a-Si:H	Color TV	Lab demo
Fujitsu	6.0	240x960	a-Si:H	Color TV	Lab demo
GE	8.8	1024x1024	a-Si:H	Color Graphic	Prototype
GEC (UK)	4.9	256x256	poly-Si	Mono Graphic	Lab demo
Hitachi	5.0	240x480	a-Si:H	Color TV	Product
	6.3	600x640	a-Si:H	Color TV	Prototype
	10.4	480x640x3	a-Si:H	Color Graphic	Prototype
Hoisden	9.5	960x960	a-Si:H	Color Graphic	Prototype
	9.7	1024x1024	a-Si:H	Color Graphic	Prototype
Litton	9.5	400x640	CdSe	Mono Graphic	Prototype
LETI	5.1	288x488	a-Si:H	Color Graphic	Lab demo
Matsushita	3.0	240x378	a-Si:H	Color TV	Product
	12.5	480x640	a-Si:H	Color TV	Lab demo
	2.3	960x1422	a-Si:H	Projection	Lab demo
Mitsubishi	10.2	450x1920	a-Si:H	Color Graphic	Lab demo
NEC	4.3	378x480	a-Si:H	Color TV	Lab demo
	12.0	240x320x3	a-Si:H	Color Graphic	Lab demo
NTT	14.0	1500x1680	a-Si:H	Color Graphic	Lab demo
OIS	3.0	372x260	a-Si:H	Color TV	Prototype
	10.0	660x680	a-Si:H	Mono Graphic	Prototype
	10.0	660x680	a-Si:H	Mono TV	Lab demo
Oki	9.0	400x640x3	a-Si:H	Color Graphic	Lab demo
Phillips	5.0	288x468	a-Si:H	Color TV	Prototype
	1.9	454x480	poly-Si	Projection	Lab demo
Sanyo	6.0	480x640	a-Si:H	Color TV	Prototype
Sarnoff Res. Ctr.	3.2	192x192	poly-Si	Color Graphic	Lab demo
Seiko Epson	2.1	240x240	poly-Si	Color TV	Product
	5.1	440x480	poly-Si	Color Graphic	Prototype
	9.5	480x960	poly-Si	Color Graphic	Lab demo
	9.4	220x320	poly-Si	Color TV	Product
Seiko Inst.	14.0	440x1950	a-Si:H	Color TV	Lab demo
Sharp	3.0	240x384	a-Si:H	Color TV	Product
	5.0	480x640	a-Si:H	Color TV	Product
	14.0	960x1284	a-Si:H	Color TV	Prototype
Stanley	6.0	440x640	a-Si:H	Color Graphic	Prototype
Toshiba	4.0	220x480	a-Si:H	Color TV	Product
	6.5	440x720	a-Si:H	Color TV	Prototype
	9.5	1024x1024	a-Si:H	Color Graphic	Lab demo
Toshiba/IBM	14.3	1100x1440	a-Si:H	Color Graphic	Lab demo

Viewing angle dependence is an inherent nature of TN LC display. Presently, the viewing angle dependence of TFT-LC devices is only acceptable for personal-viewing applications, but is not adequate for larger, multi viewer uses. The dependence on viewing angle can be minimized by optimizing cell thickness vs. LC anisotropy. Some other LC effects incorporated with AM addressing will be developed in the future which can drastically improve the viewing angle performance.

15.8 CONCLUSION

In the last few years, the AM LC device has made tremendous progress and is emerging as a strong contender to challenge the CRT. In many areas such as weight, power consumption, viewability under strong ambient light, response time, color gamut and cell brightness, TFT-LC devices have equivalent or superior performance than CRT's. TFT-LC devices still need to improve on their manufacturing cost, large size availability and viewing angle dependence to be widely accepted by users.

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